contention that "it is a matter of design choice to dispose the pipeline in between the disk drive data ports and the buffer memory data ports" for the following reasons.

Operation of the present invention is explained in the inventor's Affidavit, see paragraphs 5-8, so it will not be repeated here. (The entire Affidavit is incorporated by reference in these Remarks.) The inventor explains how elements (d) (e) and (f) of claim 1 (as labeled in the Affidavit) – the use of a common read strobe – effectively synchronizes the reading of data from the individual disk drives. When all the drives are ready, data is stored in the buffer as described in element (f). The new method further calls for inserting the redundancy logic, i.e. the data reconstruction logic (formed using a pipeline of registers in the preferred embodiment), into this data path between the disk drive data ports and the buffer memory. This technique requires a single data stream. See element (g), *viz*: "said synchronously retrieving and storing the read data elements from all of the disk drive data ports includes clocking the read data through the common pipeline so as to form a contiguous word serial data stream through the pipeline..." [emphasis added].

As the inventor explains at paragraph 8, "Once I have formed a single, contiguous word-serial data stream through the pipeline, the method calls for (h) 'concurrently computing redundant data from the read data while the read data moves through the pipeline.' If a failed drive has been identified, the computed redundant data is substituted into the data stream in lieu of the failed disk drive data. In this way, the correction is made on the fly. Moreover, the erroneous data (read from the failed disk drive) is never stored in the memory buffer."

The Searby patent teaches storing ALL the read data, including erroneous data, into the buffer memory. See the Affidavit, paragraphs 10-13, concluding as follows: "The circuitry taught by Searby thus differs from my invention in that the delay shift register 57 of figure 3 is disposed between the RAM buffer memory 40 and the external data bus (register 50) which is connected to the host. This arrangement contrasts with the architecture of my invention, as illustrated in my figure 9, which shows that a shift register 902 is disposed between the disk drive data ports (900) and the buffer memory (in figure 9, "TO CACHE").... Searby thus inserts his redundancy logic as this data is merged, i.e. after it has been buffered. Accordingly, the

Searby system requires buffering all the disk drive read data, *including the redundant data*. This is a small penalty – some 5% – in Searby's system because it contemplates 20 disk drives. My invention is directed to small RAID systems with, e.g., two drives plus one redundant drive. To buffer the redundant drive in that case, as taught by Searby, would represent a 50% increase in the buffer size, and a corresponding increase in memory cost."

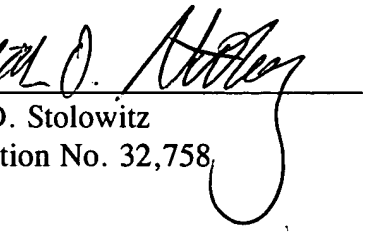
A finding of "obvious design choice" is precluded where the claimed structure and the function it performs are different from the prior art. See In re Gal, 980 F.2d 717, 25 USPQ2d 1076 (Fed. Cir. 1992). In In re Chu, the court held that placement of an SCR catalyst within the bag retainer of an emission control apparatus was not merely a "design choice." The modification of the prior art suggested by the Examiner was not supported. The court said, *inter alia*, "First, there is no teaching or suggestion in the prior art that would lead one of ordinary skill in the art to modify the [prior art] structure to place the SCR catalyst within a bag retainer as opposed to between two filter bags as disclosed in [the reference]." And, the court referred to the applicant's technical evidence that also would militate against a conclusion that the placement of the SCR catalyst was merely a design choice. In re Chu, 66 F.3d 292, 36 USPQ2d 1089 (Fed. Cir. 1995 (obviousness rejection, affirmed by the BPAI, *reversed* by the court)). In the present case, the inventor's Affidavit explains why the modification of the prior art suggested by the Examiner would not work; it would render the prior art apparatus inoperative. Affidavit paragraphs 14-17, inclusive.

The Examiner supports the proposed rearrangement of the Searby system on the ground that it would "enhance the error checking and data reconstructing of Searby's system." The enhancement is taught by the present applicant; the proposed modification is no more than hindsight reconstruction. Moreover, general motivational statements, e.g. to improve performance, are improper. As the Patent Office recently stated, "The motivation, improve efficiency, is too general because it could cover almost any alteration contemplated of Reference A and does not address why this specific proposed modification would have been obvious." USPTO, *Formulating and Communicating Rejections Under 35 U.S.C. 103 for Applications Directed to Computer-implemented Business Method Inventions*, part V. Examples of Improper Rejection under 35 U.S.C. 103, Example 17.

For the foregoing reasons, applicant respectfully contends that the Examiner has not provided a *prima facie* basis for the obviousness ground of rejection of claims 1-19. All of the remaining claims are patentable essentially for the reasons explained with reference to claim 1. This application therefore should be allowed and passed to issue.

Respectfully submitted,

Michael C. Stolowitz

By: 

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